REMARKS

Reconsideration and allowance are respectfully requested in light of the above amendment and the following remarks.

Each of the independent claims has been amended to emphasize that the purpose of the operation of adding at least one predetermined bit to the beginning of one of the code blocks is so that each of the code blocks has one of the CRC-bits as a last bit thereof, as one of the constitutional differences between the present amended claims and USPN 5844918 to Kato.

Claims 34-51 stand rejected under 35 USC 103 as obvious over USPN 5844918 to Kato. The Applicants respectfully traverse.

The Advisory Action of December 15, 2004 proposes to combine Kato's prior art Fig. 2 with Kato's invention embodiment of Figs. 5 and 7. The Advisory Action stated that "the purpose of the present invention includes segmenting the concatenated code block (sic- transport block) into code block (sic- code blocks) where each of the code blocks has one of the CRC bits as a last bit thereof....Kato teaches (Figure 2b), for example, to add dummy data to make the packets of the same length and then in Fig. 2c the CRC is attached. See Kato: Abstract, Figure 2a-e, Figure 5a-d, Figure 7a-d,col. 3, lines 25-30 and cols. 9-10." Thus, the Advisory Action relies on Kato's prior art Fig. 2 which uses dummy data. But the Applicant states in the background section of the present

application that Applicant's admitted prior art Fig. 5 involves use of known (dummy) data. Thus, the cited aspect of Kato's prior art Fig. 2 does not add anything to the admitted prior art cited in Applicant's background of the invention section.

It is submitted that the present rejection has several weaknesses.

The first weakness is that, even if Kato's Fig. 5 embodiment were modified to include the features of Kato's prior art system of Fig. 2, this still would not achieve the subject matter of the present independent claims.

This is because Kato's Fig. 2 discloses, in Fig. 2b, first, adding dummy data to make the packets of the same length, and thereafter, in Fig. 2c, attaching the CRC to the packets. Thus, the CRC bits are added after the dummy data is inserted. In contrast, in the present claimed invention, the CRC-bits are added to the transport blocks prior to the addition of the at least one predetermined bit to the beginning of one of the code blocks.

Further, the purpose of adding at least one predetermined bit of the present claims is so that the CRC bit will be placed as a last bit of each of the code blocks, as amended in each of the present independent claims. On the other hand, the purpose of adding the dummy data in Kato's combined Figs. 2 and 5 would be to make the length of the packets before CRC addition equal (see Fig.

2b).

Accordingly, due to at least these significant differences between the present claims and Kato's combined Figs. 2 and 5 with respect to the different orders of processing and configuration and the different purposes of inserting the predetermined bit and the dummy data, it is submitted that, even if Kato's Figs. 2 and 5 were combined, the present claims would still not be achieved by this combination and thus the present claims are allowable over Kato.

In addition to the above difference, further significant patentable differences exist between the present claims and Kato as follows.

Each of the present independent claims patentably distinguishes over Kato in that, in the present claims, the operations are:

(1) attach CRC bits to plural transport blocks which were previously formed by dividing transmission data into plural transport blocks (it is noted that the claims do not recite the operation of dividing the transport data into the plural transport blocks),

(2) concatenate the transport blocks, and

(3) segment the concatenated transport block into code blocks including adding a predetermined bit to the beginning of one of the code blocks so that each code block has one of the CRC bits as a last bit thereof.

Then, each code block is error correction encoded (it is noted that the claims do not recite the operation of error correction encoding).

In contrast, in Kato, the steps are:

(1) perform error correcting encoding on the basic data as a whole to provide an error correcting code including the basic data and a parity code,

(2) divide the error correcting code into fixed length blocks,

(3) add CRC bits to the end of the divided fixed length blocks, and

(4) add packet headers, concatenate and transmit.

From the above, it is seen that the present claimed invention operates on the basic data previously divided into transport blocks, concatenates the transport blocks, and thereafter performs a segmenting step of dividing the concatenated data into code blocks. In contrast, Kato discloses only division of the error correcting code into fixed length blocks, no step of segmenting into code blocks, and no step of division of any kind after the concatenation operation of Fig. 5d.

Thus, for this additional reason, it is submitted that even if Kato's Figs. 2 and 5 were combined as proposed in the Advisory Action, this still would not have achieved the Applicant's claimed invention and the present claims are allowable over Kato.

Further, the Applicant submits that it would not have been obvious to combine Kato's Figs. 2 and 5 systems. This is because Kato's invention of Fig. 5 is directed to operating without execution of FEC on a packet-by-packet basis, whereas Kato's prior art Fig. 2 system executes FEC on a packet-by-packet basis. Incidentally, the Applicant notes that the present claimed invention is directed to executing error correcting coding processing on a code block-by-code block basis and thus is different in this point from Kato's Fig. 5. Further, the purpose of Kato's invention is to achieve proper operation even where the data to be subjected to the FEC operation and a data packet are different in length. See col. 33, lines 16-28. Kato's invention of Fig. 5 divides an error correcting code consisting of basic data complete with a parity code into smaller data segments, whereas Kato's prior art Fig. 2 divides the basic data without a parity code appended thereto into smaller segments. There is no need to add dummy data in Kato's Fig. 5 invention. Thus, there is no suggestion or motivation for combining the use of dummy data of Kato's Fig. 2 into Kato's Fig. 5.

In addition to the above, the Applicant submits that the present claims are allowable over Kato for the reasons set forth in the Response filed November 30, 2004. That Response pointed out that the orders of the operations in the present claimed invention

and Kato are different, and the purposes of the operations are different. It would not have been obvious to rearrange the order of the steps in Kato to achieve the present claimed invention, and there is no motivation to make such a modification of Kato's system.

Further, the previous Response noted that the present claimed invention is directed to solving the problem discussed at application page 1, line 9 through page 3, line 20 and illustrated in Fig. 5. The Applicant's representative noted during the personal interview of November 29, 2004 how the present invention solves the problem illustrated in Fig. 5. In contrast, Kato deals with a different problem, as discussed at col. 3, lines 5-14, and Kato solves this problem as discussed at col. 3, lines 16-35. Kato's Figs. 2 and 5 show no recognition of the problem addressed by the present invention, and do not teach a solution to this problem.

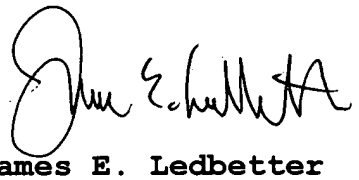
It is noted that claims 35 and 47 recite that the predetermined bit is added when a number of bits of the concatenated transport block is not an integer multiple of the number of the code blocks. This feature provides a further basis for the allowance of these two claims.

For the above reasons, it is submitted that each of the

present claims is allowable over Kato. A notice of allowance is respectfully solicited.

If any issues remain that may be best resolved through a telephone communication, the examiner is requested to telephone the undersigned at the local Washington, D.C. telephone number listed below.

Respectfully submitted,



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